

Name : RAJANI BISHT

Designation : Professor, Electronics Engg.

Department : Electronics Engg. HBTU Kanpur

Mobile No. : 7081300588

Area of Interest

Major Area: VLSI DESIGN, TFT CIRCUITS, RF CIRCUITS

Minor Area: Microprocessors

Personal Profile

Date of Birth : 03.03.63

Marital Status : Married

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Academic Qualifications

Sl. No.	Degree	Year	Institute/ College	University
1.	BE	1984	GEC JABALPUR	Rani Durgawati University Jabalpur
2.	ME	2000	University Of Roorkee, Roorkee	University of Roorkee, Roorkee
3.	PHD	2021	IIT Kanpur	IIT Kanpur

M.Tech. Dissertation: “A Study of VLSI Interconnect Delay Minimization Using CMOS - Repeaters”

Doctoral Dissertation: “Design of Reconfigurable Low-Noise Amplifiers for Multiband Receiver”

Experience Record

Academic:

Sl. No.	Designation	Organization	Duration
1.	Professor	HBTU Kanpur	7.08.2021 onwards
1	Associate Prof.	HBTU Kanpur	2003 to 7.08.2021
2	Assistant Prof.	HBTI Kanpur	1998 to 2003
3	Sr. Lecturer	HBTI Kanpur	18 Oct 1993 to 1998
4	Lecturer	Govt. Engg. College Bhopal	Nov 1990 to 1991
5	Lecturer	Govt. Women's Polytechnic Bhopal	1987 to 1990
6	Lecturer	Govt. Polytechnic Durg	Oct. 1984 to July 1987

Scientific:

Sl. No.	Designation	Organization	Duration
1	Senior Project Associate	I.I.T. KANPUR	August 1991 to 1992

Teaching Records

Courses Taught at PG Level:

- VLSI SYSTEM DESIGN
- ADVANCED MICROPROCESSORS
- SOLID STATE SEMICONDUCTOR DEVICES
- ADVANCED SEMICONDUCTOR DEVICES

Courses Taught at UG Level:

- MICROPROCESSORS
- VLSI TECHNOLOGY
- VLSI DESIGN
- DIGITAL INTEGRATED CIRCUITS
- ELECTRONICS CIRCUITS & DEVICES
- INTEGRATED CIRCUITED & DEVICES
- MICROELECTRONICS
- ANTEENA & WAVE PROPAGATION
- INDUSTRIAL INSTRUMENTATION
- COMPUTER AIDED DESIGN OF ELECTRONIC CIRCUITS
- COMMUNICATION SYSTEM PRACTICE
- PC HARDWARE
- ADVANCED SEMICONDUCTOR DEVICES
- DIGITAL SYSTEM DESIGN USING VHDL

Invited lectures at Other Organizations

- “VLSI Design & Testing” at Institution of Engineers, Kanpur Chapter on Feb 15th, 2004.
- MPEC Kanpur “Overview on VLSI Design”
- AITH Kanpur “ Overview on VLSI Design”

Administrative Experience

Administrative Work:

- 1988-1990 2nd LT. NCC OFFICER GOVT. WOMEN'S POLYTECHNIC BHOPAL
- 1989-1990 WARDEN GOVT. WOMEN'S POLYTECHNIC BHOPAL
- 2005 WARDEN NGH HBTI KANPUR
- Warden GH-IV HBTI Kanpur
- Head Electronics(two terms) HBTI Kanpur
- Warden Gangotri Hostel HBTU Kanpur
- Associate Dean Academic HBTU Kanpur
- Warden Kaveri Hostel HBTU Kanpur
- Additional COE HBTU Kanpur

Professional Committee Work:

- 2001, Member, Syllabi making committee, curriculum development of UPTU syllabus of Electronic & Communication, HBTI KANPUR
- 2004, Member, Syllabi making committee, curriculum Revision of UPTU syllabus of Electronic & Communication, HBTI KANPUR
- 2004, Member, Syllabi making committee, curriculum development of Polytechnic syllabus of Electronic & Communication, IRDT, KANPUR
- Member BOS, HBTI Kanpur
- Member Women Study center HBTU Kanpur
- Member ICC Committee
- Member 30-hr course for women health
- Member BOE, HBTU KANPUR

Membership of Professional Bodies

Associate Member/Institution of Electronics & Telecommunication Engineers/M138582
Student Member IEEE/ Membership no. 94904765

Research Guidance Guided many U G projects and M. Tech Theses

S. No.	Year	Title of M tech Thesis	Name of Student
1.	2004	Single Precision 32 Bit Pipeline Floating Point Addition & Subtraction in VHDL	Ms. Richa (740/02)
2.	2004	Automatic Test Pattern Generator for Sequential Circuits	Amit Kumar (733/02)
3.	2005	Analog Technique for MOS and TFT Circuits	Sunil Kumar Yadav (720/03)
4.	2005	Process Automation System for Differential Pressure Control of Propellant Tanks in Liquid Rocket Stages	Man Mohan Vaishya (721/03)
5.	2006	Analysis of Tradeoff in CMOS Differential Amplifier	Ajay Bharti (745/04)
6.	2007	Design of I/O Buffer (Slew Rate Controlled) in 65nm CMOS Process	Manoj Kumar Tiwari (721/05)
7.	2007	Analysis of Impact of Kink effect on poly-silicon TFT Analog Circuit & its reduction	Manish Agarwal (702/05)
8.	2010	Analysis and Characterization of Gate Diffusion Input	Arun Prakash Singh (709/07)
9.	2010	Design and Implementation of Fast Adders Using VHDL	Nishi Chandra (729/08)

		and FPGA	
10.	2011	Design of 16 -bit Microprocessor using VHDL	Abhai Shankar Chaurasia (734/09)
11.	2011	Design of Adder using Quaternary Signed Digit Number System	Vishal Pandey (732/09)
12.	2012	Characterization of Low Power MOS SRAM Cells	Ankit Khandelwal (707/10)
13.	2012	Threshold Voltage Compensation for Analog circuit design using TFT	Geeta Awasthi (710/10)
14.	2013	Design of MOS current mode Logic Adder	Koshal Kishor Gupta (707/11)
15.	2013	Low Power CMOS full adder design	Pankaj Verma (709/11)
16.	2014	Design of 8-bit RISC Microprocessor using VHDL	Atul Kumar (723/12)
17.	2014	Floating Point Multiplier Design based on Vedic Multiplication Technique using VHDL	Pankaj Singh (726/12)
18.	2014	Performance Analysis of conventional & Double Gate (DG) MOSFET	Rajesh Kumar (729/12)
19.	2015	Leakage Power Reduction Techniques for CMOS Circuits	Kuldeep Singh (741/13)
20	2020	Design of Low-Power Reconfigurable Low Noise Amplifier for Multiband Receiver	Ashutosh Pandey (180205018)
21	2020	Design of an Ultra-Low Power Low Noise amplifier for 5 GHz Frequency Band	Nishant Kumar (180205007)
22	2021	Leakage Reduction in CMOS VLSI Circuits	Ayush Tiwari (190205006)
23	2021	Design of Low-Power Low-Noise Amplifier	Kailash Kumar (190205010)
24	2022	Design of Low Power Universal Asynchronous Receiver and Transmitter	Pranay Anand Tiwari (2002050003)

Sponsored Projects

Title	Funding Agency	Amount	Duration
“VLSI Design”,	AICTE,	Rs10.0Lacks,	Three Years

Publications (Conferences)

Sr. No.	Authors	Title of Paper	Name of Organizer (Institution)	Name of University	Conference Date and Year
1	Ashutosh Pandey, Rajani Bisht	Design of Low-Power Reconfigurable Low Noise Amplifier for Multiband Receiver	IEEE	IEEE	INOCON 2020 02-06 Nov., 2020
2	Nishant Kumar, Rajani Bisht	Design of an Ultra-Low Power Low Noise amplifier for 5 GHz Frequency Band	IEEE	IEEE	INOCON 2020 02-06 Nov., 2020
3	Rajani Bisht, S. Qureshi	“Design of Low-Power Reconfigurable Low-Noise Amplifier with Enhanced Linearity”	TENCON 2019	Kochi, Kerala	17-20 Oct. 2019
4	Abhai Shankar Chaurasia, Rajani Bisht, Manoj Kumar Shukla	“Design of 16-Bit Microprocessor using VHDL”	ETEIC-2012	Anand Engg. College Agra	April 6 th -7 th 2012
5	Rajani Bisht, B. Mazhari	“Impact of Kink Effect on Performance of Poly-Silicon based TFT Differential Amplifiers”	Asian Symposium on Information Display (ASID)	IIT Kanpur	06 in New Delhi during Oct 8 to Oct 12, 06.
3	Rajani Bisht, S Sarkar, R P Agarwal	“VLSI interconnect delay minimization using CMOS inverters”	IIT, Roorkee	IIT, Roorkee	Proceedings of All India Seminar on Recent Trends in VLSI, 29 th -30 th September 2001

Publications (Journals)

S. No.	Authors	Title of paper	Journal	year
1	Rajani Bisht, M.J. Akhtar, S. Qureshi	“Design of Reconfigurable Multi-Band Low-Noise Amplifiers for 802.11ah/b/g and DCS-1800 Applications”	International Journal of Electronics and Communications, (2020), doi: https://doi.org/10.1016/j.aeue.2020.15320	2020
2	Nishant Kumar, Rajani Bisht	“A review of an ultra-low-power LNA with High power gain for 5-GHz frequency band applications”	International Journal of Advances in Engineering and Management (IJAEM), Volume 2, Issue 1, pp : 324-326 ISSN: 2395-5252 DOI: 10.35629/5252-45122323	2020
3	Ashutosh Pandey, Rajani Bisht	“A review of different techniques used to design a low- noise amplifier”	International Journal of Advances in Engineering and Management (IJAEM), Volume 2, Issue 1, pp: 140-144 ISSN: 2395-5252 DOI: 10.35629/5252-451223	2020
4	Ashutosh Pandey, Rajani Bisht	“Design of Low-Power Reconfigurable LNA for Multi-Standard Receiver”	International Journal for Research in Applied Science and Engineering Technology, Volume 8, Issue VI June 2020, pp:2447-2451 ISSN: 2321-9653 DOI: http://doi.org/10.22214/ijras et.2020.6392	2020
5	Ayush Tiwari, Rajani Bisht	“Leakage Power Reduction in CMOS VLSI Circuits using Advance Leakage Reduction Method ”	International Journal for Research in Applied Science and Engineering Technology (IJRASET) Page No: 962-966, ISSN : 2321-9653.	2021
5	Kailash Kumar , Rajani Bisht	“A Review on Low-Noise Amplifier”	International Research Journal of Modernization in Engineering Technology and Science (IRJMETS), Volume:03/Issue:06/June-2021.	2021
6	PranayAnand Tiwari, Rajani Bisht	“Design of Low Power Universal Asynchronous Receiver and Transmitter”	International Journal of Engineering Research & Technology (IJERT) ISSN: 2278-0181 IJERTV11IS090097 (Vol. 11 Issue 06, September 2022)	2022